Revision History

Version	Description of Changes	Revised By	Date
001	Initial Release	J. Feuerstein	5/15/2018

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1 Purpose

This Design-in Guide compliments the hardware manual to help you get started on integrating the phyCORE-AM57x SOM into your own system. It provides recommendations on power supply selection, routing, placement, and other topics directly related to designing your own customer carrier board design.

2 Design Guidelines

2.1 Power

The SOM operates from two primary power sources, VCC_5V0_IN and VCC_3V3_IN, and an optional off-chip RTC power source VBAT. In addition, The SOM provides a 3.3V power supply, VDD_SD, as an SD card power source on the carrier board.

For proper operation, connect at least as many GND pins to ground as power supply pins. As a general design rule, we recommend connecting all GND pins located next to signals which are being used in the application circuitry. Connecting the neighboring GND pins provides a low impedance return path, improves signal quality, and reduces EMI. For maximum EMI performance all GND pins should be connected to a solid ground plane.

All power signals are located on the X2 connector, while the ground pins are distributed across both X1 and X2 connectors. See Table 1 and Table 2 below for pin numbers and specifications.

Table 1: X1 Ground Pins

Signal	I/O	Pins	Description
GND	Out (Required)	A4, A9, A14, A19, A24, A29, A34, A39, A44, A49, A54, A59, A64, A69, A74, A79, B2, B7, B12, B17, B22, B27, B32, B37, B42, B47, B52, B57, B62, B67, B72, B77	Ground

Table 2: X2 Power Pins

Signal	I/O	Pins	Description
VCC_5V0_IN	In (Required)	B6	+5.0V ±5%
VCC_3V3_IN	In (Required)	A1, A2, A3, B1, B2, B3	+3.3V ±5%
VBAT	In (Optional)	A6	If RTC backup required, voltage should be between ~1.0V and VCC_3V3_IN supply voltage
GND	Out (Required)	A5, A10, A15, A20, A23, A26, A35, A40, A45, A50, A55, A60, A65, A70, A75, A80, B5, B11, B16, B19, B22, B25, B28, B31, B34, B37, B48, B53, B61, B66, B71, B76	Ground
VDD_SD	Out	A4	+3.3V, max 300mA

2.1.1 Minimum Power Up Requirements

Connect all the VCC_3V3_IN and VCC_5V0_IN pins and the matching number of GND pins for minimum SOM power up. The VBAT pin can be left floating if not used in the design.

2.1.2 Regulator Recommendations

PHYTEC recommends using TI's TPS54531 switching regulator to generate VCC_3V3_IN and VCC_5V0_IN required by the SOM. This regulator is a good general-purpose solution for many system configurations, but other regulators more suited to specific system requirements may also be used.

It is important to do a power analysis to determine how much current your system requires. The phyCORE-AM57x Carrier Board provides an easy access current shunt to measure SOM current under various operating conditions as part of your system power analysis. Use your maximum measured SOM current combined with the current requirement for your carrier board peripheral devices to size your regulator's current output appropriately.

2.1.3 Sequencing

Pay special attention to the power sequencing of your power supplies. VCC_3V3_IN must be available to the SOM before or at the same time as VCC_5V0_IN.

All other power rails required by devices and components on your Carrier Board need to be sequenced with X_EXT_PWR_ON (which is a 3.3V active high signal) located on X2-B10. It is recommended to implement regulators or power switch devices with an enable input driven by X_EXT_PWR_ON. This will ensure that the SOM is properly powered before enabling external power supplies on your Carrier Board design.

2.1.1 X_PWRON Power-On Control

The X_PWRON signal must be toggled low momentarily to properly trigger a power-up event and bring up the SOM. The PMIC requires this ON request and will not trigger the power-up sequence otherwise. Note that X_PWRON cannot remain low longer than the PMIC long-press delay (~4 seconds by default), as this will trigger a "long press" interrupt which will then switch the system off. The TPS6590374 PMIC datasheet can be referenced for further details regarding ON requests and the PWRON pin.

X_PWRON can be handled manually with a button or switch solution tying the signal to ground when pressed. If a manual power-on trigger is not possible for your application, a circuit to toggle this signal at power-up for an automatic response can be implemented.

An application note providing an example circuit for automatic power-up is available here:

https://wiki.phytec.com/display/public/PRODUCTINFO/Application+Note%3A+AM57x+Automatic+Power-On+Event+at+Power+Up

2.1.2 Safe Shutdown and Sudden Power Loss

Like a PC, a sudden power loss can result in a corrupted filesystem that renders your system unable to boot. When possible, initiating an OS controlled shutdown procedure is advised. Under Linux a **poweroff** or **shutdown** command will safely shutdown the system, allowing subsequent safe removal of power.

If sudden power loss is a concern in your system then consider designing a battery backup or other similar failsafe solution. An appropriate battery backup provides enough temporary power for the system to complete a safe shutdown. The safe shutdown should be triggered via an interrupt to the processor when primary system power loss is detected.

2.2 AM572x vs. AM571x Differences

If using a phyCORE-AM57x SOM populated with an AM571x variant, there are several differences that have an impact on the phyCORE-AM57x design integration. The major differences are listed in the sections below.

2.2.1 phyCORE-AM57x Pin Out

Table 3: AM572x vs. AM571x phyCORE Pin Out Differences

	AM572x		AM571x	
Pin #	**Signal**	**Level**	**Signal**	**Level**
X1-A32	X_KBD_ROW2	3.3V	**CSI2_0_DY3**	**1.8V**
X1-A33	X_KBD_ROW3	3.3V	**Not Connected**	**-**
X1-A45	X_WAKEUP2	3.3V	**DDR1_CSN1**	**1.35V**
X1-A65	X_VIN3A_D4	3.3V	**CSI2_0_DY1**	**1.8V**
X1-A66	X_VIN3A_D5	3.3V	**Not Connected**	**-**
X1-A67	X_VIN3A_D6	3.3V	**CSI2_0_DY0**	**1.8V**
X1-A68	X_VIN3A_D7	3.3V	**Not Connected**	**-**
X1-A75	X_VIN3A_CLK0	3.3V	**CSI2_1_DX2**	**1.8V**
X1-B33	X_KBD_ROW0	3.3V	**Not Connected**	**-**
X1-B34	X_KBD_ROW1	3.3V	**Not Connected**	**-**
X1-B40	X_EHRPWM1B	3.3V	**Not Connected**	**-**
X2-A48	X_WAKEUP1	3.3V	**DDR1_ODT1**	**1.35V**
X2-B29	X_PCIE_TXN1	1.8V	**Not Connected**	**-**
X2-B30	X_PCIE_TXP1	1.8V	**Not Connected**	**-**
X2-B32	X_PCIE_RXN1	1.8V	**Not Connected**	**-**
X2-B33	X_PCIE_RXP1	1.8V	**Not Connected**	**-**
X2-B56	X_EHRPWM1A	3.3V	**Not Connected**	**-**

2.2.2 DDR

The second EMIF controller is not supported on the AM571x. Therefore, only one DDR bank can be populated on the phyCORE-AM57x SOM utilizing the EMIF1 controller.

2.2.3 Display

The VOUT1, VOUT2, and VOUT3 interfaces are not supported at 3.3V for the AM571x (they are only qualified for 1.8V operation). Since these ports are directly powered by 3.3V on the phyCORE-AM57x SOM, display is not supported via these ports.

2.2.4 Camera

The VIP2 and VIP3 ports are not supported on the AM571x. The AM571x VIP1 ports (vin1a/vin1b and vin2a/vin2b) are remapped to the AM572x VIP2 ports (vin3 and vin4).

Although the AM571x supports Camera Serial Interface 2 (CSI2), the phyCORE-AM57x SOM does not bring out all of the pins for this interface. Therefore, the CSI2 interface is not supported on the phyCORE-AM57x SOM.

2.2.5 PCIe

The second lane at X_PCIe_TXN1/X_PCIE_TXP1 and X_PCIe_RXN1/X_PCIE_RXP1 is not connected on the AM571x.

2.2.6 GPIO

The following GPIO channels are not supported by the AM571x: **GPIO1_[1:0]** / **GPIO2_[31:30]** / **GPIO3_[27:0]**

2.3 Boot Pins

During the power-on reset cycle the operational system boot mode of the AM57x processor is determined by the configuration of the SYSBOOT [15:0] pins. These signals are named X_GPMC_ADxx/SYSBOOTxx at the phyCORE connector. The pull-up and pull-down resistors populated on the SOM set the default sysboot [15:0] configuration to 0b1000000100100010.

Table 4 describes the function of the SYSBOOT signals.

Table 4: Sysboot Signals Description

Signal	Description
sysboot[15]	Must be pulled up for proper device operation.
sysboot[14]	Must be pulled down for proper device operation.
sysboot[13:10]	Configure the GPMC interface when booting from XIP/NAND memory on GPMC.
sysboot[9]	Must be pulled down for proper device operation.
sysboot[8]	Must be pulled up for proper device operation.
sysboot[7:6]	Sector offset for the location of the redundant SBL images in QSPI.
sysboot[5:0]	Select interfaces or devices for the booting list.

The SYSBOOT signals are latched and sampled after nPORZ. These signals can be used for other purposes after boot. To modify the default SYSBOOT configuration, use 1k pull-up, or pull-down resistors on your Carrier Board to override the SOM settings. When adding a pull-up, ensure the signal is pulled up to the 3.3V power rail enabled by the X_EXT_PWR_ON signal. See power sequencing section for more information on the proper usage of this signal. In general, only the SYSBOOT [5:0] pins need to be modified to adjust the desired boot mode.

Table 5 shows the different boot device orders, which can be selected by configuring the six boot-order configuration pins, X_GPMC_AD[5:0]/SYSBOOT [5:0] of the phyCORE-AM57x.

Table 5: Boot Device Order

SYSBOOT[5:0]	First Device	Second Device	Third Device
0b000000	USB	eMMC	
0b000001	USB	NAND	
0b000010	USB	SD	eMMC
0b000011	USB	SATA	SD
0b000100	USB		XIP
0b000101	SD	XIP	
0b000110	SD	QSPI_1	
0b000111	SD	QSPI_4	
0b001010	SD	Fast XIP	
0b010000	USB		
0b0101XX	SD	USB	
0b0110XX	SD	USB	
0b100000	eMMC	USB	
0b100001	NAND	USB	
0b100010[1]	**SD**	**eMMC**	**USB**
0b100011	SATA	SD	USB

[1] Default SOM boot configuration

0b100100	XIP	USB	
0b100101	XIP	SD	USB
0b100110	QSPI_1	SD	USB
0b100111	QSPI_4	SD	USB
0b110000	SD		
0b110100	SATA		
0b110101	XIP		
0b110110	QSPI_1		
0b110111	QSPI_4		
0b111000	eMMC		
0b111001	NAND		
0b111010	Fast XIP		
0b111011	eMMC (boot partition)		

Table 6 lists the boot interfaces and the pin muxing supported by the ROM for booting.

Table 6: Pin Multiplexing According to Boot Peripheral

Boot Device	Boot Interface	Pads	MuxMode	SOM Signals
eMMC	MMC2	gpmc_a[22:19]	0x1	MMC2_DAT[7:4]
		gpmc_a[23]		MMC2_CLK
		gpmc_a[27:24]		MMC2_DAT[3:0]
		gpmc_cs[1]		MMC2_CMD
SD	MMC1	mmc1_clk	0x0	X_MMC1_CLK
		mmc1_cmd		X_MMC1_CMD
		mmc1_dat[3:0]		X_MMC1_DAT[3:0]
NAND	GPMC	GPMC on CS0	0x0	GPMC on CS0
XIP	GPMC	GPMC on CS0	0x0	GPMC on CS0, per wait signal setting SYSBOOT[10]
SATA	SATA	sata1_txp0	-	X_SATA_TX+
		sata1_txn0		X_SATA_TX-
		sata1_rxp0		X_SATA_RX+
		sata1_rxn0		X_SATA_RX-
QSPI_1/QSPI_4	QSPI_1	gpmc_a[18]	0x1	X_QSPI1_SCLK
		gpmc_a[17:14]		X_QSPI1_D[3:0]
		gpmc_a[13]		X_QSPI1_RTCLK
		gpmc_cs[2]		X_QSPI1_CS0
USB	USB1	usb1_dp	-	X_USB1_DP
		usb1_dm		X_USB1_DM

2.4 SOM Flash Configuration

The phyCORE-AM57x SOM can be configured to use NAND flash or eMMC as nonvolatile memory storage device. Both of these configurations cannot be implemented at the same time; it is only possible to implement either NAND flash or eMMC. The footprints for each of these memory devices share the same area on the PCB, as well some overlapping signals from the processor.

2.4.1 NAND

The following components must be populated when implementing NAND flash:

U14, R101-R106, R222-223, R243-250, R182, R229, C3, C35, C294

The following components should be removed when implementing NAND flash:

U5, R224, C372, C150-151

2.4.2 eMMC

The following components must be populated when implementing eMMC:

C148-52, C272, C320, C372, C152, U5, R224

The following components should be removed when implementing eMMC:

U14, R101-R106, R222-223, R243-250, R182, R229

2.5 General Signal Routing Guidelines

- Pay special attention to signal placement, trace impedances, maximum trace length, and trace length tolerances when routing SOM signals.
- Place and route high-speed signals, such as USB3.0, SATA, PCIE, HDMI, ETHERNET, etc., before placing and routing any other interfaces. This is recommended to ensure that the stricter trace lengths and length matching requirements of these interfaces are met.
- Place and route the remaining interfaces after the high-speed interfaces are completely routed.
- Please note that all the single ended and differential impedances have a ±10% tolerance.

2.5.1 Additional Considerations and Recommendations

2.5.1.1 Audio

Add series termination resistors (recommended to use 22Ω) to the digital lines of the audio interface to improve signal integrity by mitigating overshoot and undershoot. The following table describes the preferred location of these series termination resistors.

Table 7: Audio Termination Resistor Locations

Signal	Resistor Location
X_XREF_CLK0	Near the phyCORE connector pin
X_MCASP1_AXR14	Near the phyCORE connector pin
X_MCASP1_FSX	Near the Audio Codec pin
X_MCASP1_AXR15	Near the Audio Codec pin
X_MCASP1_ACLKX	Near the Audio Codec pin

2.5.1.2 RGMII1

Refer to the following list for recommendations on implementing the RGMII interface:

- Place the Ethernet PHY as close as possible to the SOM connector and keep the trace lengths of the RGMII signals as short as possible.
- Add a 10kΩ pull-down resistor on any unused input or I/O signal on this interface if it is not connected to a PHY.
- Avoid any cuts in the ground plane or other references planes within the RGMII routing region.
- Place termination resistors (recommended to use 33Ω) near the PHY on all of the X_RGMII1_RX* signals.
- The MDIO clock and data signals do not need to be matched as strictly as RGMII. However, it is recommended to route these together and keep them length matched within 100 mils.
- RGMII v2.0 Timing Requirements (shown in the table below) specify that the clock and data will be generated simultaneously by the transmitting source, which requires a skew be introduced between clock and data.

Table 8: RGMII v2.0 Timing Requirements

Parameter	Minimum	Typical	Maximum	Units
Data to clock output skew at transmitter	-500	0	500	ps
Data to clock output skew at receiver	1	1.8	2.6	ns

The skew can be introduced with additional PCB trace delay on the carrier board or by adjusting the internal delay settings at the phy or processor. However, please note that an internal delay may not be available on the selected ethernet phy or it may not have sufficient adjustment to account for the required skew. The X_RGMII1_RXC signal has been routed with an additional trace delay on the SOM to help meet these timing requirements.

- Ensure signals are properly length matched to meet RGMII timing specifications. The following tables show the signal groups (TX vs. RX) that should be length matched and the trace length of each signal on the SOM. It is recommended to length match he control and data signals within 350 mils, and then the trace length of the clock should be the average length of these control and data signals plus an additional 1.8ns delay.

Table 8: RGMII1 TX Length Matching Recommendation

Signal Name	SOM Trace Length (Mil)	Match Group	Recommended Length Match
X_RGMII1_TXC	761	Transmit	AVERAGE_LENGTH(TXCTL, TXD0, TXD1, TXD2, TXD3) + 1.8ns
X_RGMII1_TXCTL	804	Transmit	350 Mils
X_RGMII1_TXD0	576	Transmit	
X_RGMII1_TXD1	501	Transmit	
X_RGMII1_TXD2	483	Transmit	
X_RGMII1_TXD3	484	Transmit	

Table 9: RGMII1 RX Length Matching Recommendation

Signal Name	SOM Trace Length (Mil)	Match Group	Recommended Length Match (Mil)
X_RGMII1_RXC	3426	Receive	AVERAGE_LENGTH(RXCTL, RXD0, RXD1, RXD2, RXD3) + 1.8ns
X_RGMII1_RXCTL	627	Receive	350 Mils
X_RGMII1_RXD0	544	Receive	
X_RGMII1_RXD1	507	Receive	
X_RGMII1_RXD2	658	Receive	
X_RGMII1_RXD3	652	Receive	

The recommended clock trace length on a carrier board is calculated using the following equation:
(Average total length of control/data signals on SOM) + (Average total length of control/data signals on Carrier Board) + (1.8ns delay) – (Clock Trace Length on the SOM)

Reference the equations below to determine the recommended clock length when implementing a physical delay. The 1.8ns was translated to an estimated length using the general rule of 165ps/inch. However, the actual physical trace delay will vary depending on the PCB stackup, materials, etc…

Transmit Clock Length Calculation with Physical Trace Delay:
(569.6 mils) + (Average total length of control/data signals on Carrier Board) + (10900 mils) – (761 mils)

Receive Clock Length Calculation with Physical Trace Delay:
(597.6 mils) + (Average total length of control/data signals on Carrier Board) + (10900 mils) – (3426 mils)

The skew between the clock and each individual data and control signal should not fall below the 1ns minimum or exceed the 2.6ns maximum.

2.5.1.3 LCD

NOTE: 22R series termination resistors on the LCD display signals (X_VOUT2…) are recommended to reduce undershoot and overshoot that may damage the LCD panel. These should be placed as close as possible to the phyCORE connector pins.

2.6 High-Speed Differential Signal Routing Guidelines

2.6.1 General High-Speed Differential Guidelines

- Route differential pairs on the same layer and implement proper trace width and spacing to yield the recommended differential impedance value.
- Spacing between the differential pairs and other traces should be at least twice the distance between the inter-pair spacing.
- Avoid routing high-speed signals near other high-frequency signals (such as crystals, oscillators, switching regulators, clock signals, etc…).
- Route signals over an adjacent, solid ground reference plane. Ensure there are no layers between the routing layer and reference layer.
- Avoid routing across a gap or cut-out in the reference plane or across different reference planes. Cuts in the reference plane should be avoided in general.
- Minimize discontinuities on the signal path (such as stubs) and avoid placing test points, external components like 0Ω resistors, or any other components that are not required when possible.
- Surface-mount receptacles are preferred over through-hole connectors, as signals can be routed on the top layer of the PCB without introducing vias to the signal path. If through-hole pins are necessary, it may be beneficial to route signals on the bottom layer to prevent the through-hole pin from behaving as a stub.
- The number of vias on the differential pairs should be minimized, avoid routing through vias when possible. If necessary, each signal of the differential pair should be routed through matching number of vias. In the case of multiple differential lanes in the same interface, all lines should have the same number of vias.
- Avoid sharp bends on differential lanes.
- Minimize total trace length.

2.6.2 USB2.0

- DP/DM trace lengths should be matched and should be no more than 4 inches in total length (SOM + Carrier Board). Table shows the length of the USB2.0 traces on the SOM and required constraints.
- Route DP/DM traces close together and in parallel for noise rejection, and within 50 mils in length of each other.

Table 10: USB2.0 Layout Constraints

Signal Name	Length (Mil)			Length Matching (Mil)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace			
X_USB1_DP	906	4000	3101	50	45	90
X_USB1_DM	911	4000	3089		45	
X_USB2_DP	661	4000	3339	50	45	90
X_USB2_DM	661	4000	3339		45	

2.6.3 USB3.0

- Minimize the distance between AC capacitors (TX only) and common mode filters (CMF).
- Minimize the distance between common mode filters (CMF) and ESD protection devices.
- Minimize the distance between ESD protection devices and USB connectors.
- Ensure there are no cuts in the ground plane within the USB3.0 routing region, with the exception of cut-outs in the ground reference layer directly underneath the AC capacitors, ESD devices, and common mode filters to minimize additional capacitance.

Table 11: USB3.0 Layout Constraints

Signal Name	Length (Mil)			Length Matching (Mil)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace			
X_USB1_DP	899	3500	2601	6	45	90
X_USB1_DM	911	3500	2589		45	
X_USB_RXP0	737	3500	2763	6	45	90
X_USB_RXN0	733	3500	2767		45	
X_USB_TXP0	774	3500	2726	6	45	90
X_USB_TXN0	775	3500	2725		45	

2.6.4 SATA

- The AC coupling capacitors required on SATA signals are implemented on the SOM, therefore no additional capacitors are required on the carrier board.

Table 12: SATA Layout Constraints

Signal Name	Length (Mil)			Length Matching (Mil)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace			
X_SATA_TX+	624	3050	2426	5	60	100
X_SATA_TX-	624	3050	2426		60	
X_SATA_RX+	543	3050	2507	5	60	100
X_SATA_RX-	545	3050	2505		60	

2.6.5 PCIe

- It is recommended to use an external clock generator to provide a clock to the PCIe reference input (LJCB_CLKN and LJCB_CLKP) via X_PCIE_REFCLKN and X_PCIE_REFCLKP in addition to any PCIe device(s). The external clock must be a high-quality, low-jitter differential 100MHz clock source compliant to the PCIe REFCLK AC specifications. We recommend using the PI6C557-03 clock generator, which is implemented on the PHYTEC RDK design.

- The AC coupling capacitors required on PCIe transmit and clock signals are implemented on the SOM. Therefore, no additional capacitors are required on the carrier board.

Table 13: PCIe Layout Constraints

Signal Name	Length (Mil)			Length Matching (Mil)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace			
X_PCIE_TXP0	700	4700	4000	5	60	100
X_PCIE_TXN0	702	4700	3998		60	
X_PCIE_RXP0	645	4700	4055	5	60	100
X_PCIE_RXN0	649	4700	4051		60	
X_PCIE_TXP1	594	4700	4106	5	60	100
X_PCIE_TXN1	598	4700	4102		60	
X_PCIE_RXP1	632	4700	4068	5	60	100
X_PCIE_RXN1	628	4700	4072		60	

2.6.6 HDMI

- The HDMI interface consists of three buses, TDMS, I^2C, and CEC. The I^2C and CEC buses are low speed and do not require any special layout considerations.
- Minimize the distance between common mode filters (CMF) and ESD protection devices.
- Minimize the distance between ESD protection devices and HDMI connectors.

Table 34: HDMI Layout Constraints

Signal Name	Length (Mil)			Length Matching (Mil)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace			
X_HDMI_D0-	435	4000	3565	5	60	100
X_HDMI_D0+	435	4000	3565		60	
X_HDMI_D1-	434	4000	3566	5	60	100
X_HDMI_D1+	433	4000	3567		60	
X_HDMI_D2-	438	4000	3562	5	60	100
X_HDMI_D2+	435	4000	3565		60	
X_HDMI_CLK-	435	4000	3565	5	60	100
X_HDMI_CLK+	435	4000	3565		60	

2.6.7 Ethernet (ETH0)

- The KSZ9031 transceiver supports HP Auto MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross over patch cable.
- Connecting the phyCORE-AM57x to an existing 10/100/1000Base-T network involves adding an RJ45 and appropriate magnetic devices in the design.
- Avoid any other signal lines crossing the Ethernet signals.

Table 4: Gigabit Ethernet Layout Constraints

Signal Name	Length (Mil)			Length Matching (Mil)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace			
X_ETH0_A+/TX0+	1062	4000	2938	10	50	100
X_ETH0_A-/TX0-	1057	4000	2943		50	
X_ETH0_B+/RX0+	1051	4000	2949	10	50	100
X_ETH0_B-/RX0-	1056	4000	2944		50	
X_ETH0_C+	1048	4000	2952	10	50	100
X_ETH0_C-	1051	4000	2949		50	
X_ETH0_D+	1079	4000	2921	10	50	100
X_ETH0_D-	1101	4000	2899		50	

3 Schematics

3.1 Connectors

The AM57x SOM is designed with two 0.5mm pitch 2x80 pin Samtec connectors. The mating connecter that should be used on the Carrier Board is from the Samtec BTH-080 family. PHYTEC recommends using the BTH-080-01-L-D-A-KTR.

3.2 Reference Schematics

Visit the PHYTEC Service Desk to request reference schematics.

4 Mechanical

The mounting holes are sized for M2.5. It is recommended to use the following mounting hardware to secure the SOM to a mating carrier board (all components should be sized for M2.5 thread sizing):

- 2x male-female standoffs with a 5mm standoff length
- 2x hex nuts
- 2x 3mm length screws
- 2x washers (thickness ≤ 0.5mm)

The dimensional drawing of the SOM, the DXF and STEP files of the SOM, the module connector datasheets and STEP files, and more can be found under the *Diagrams and Drawings* section through the link in the 'Additional Resources' section below.

5 Additional Resources

https://wiki.phytec.com/display/public/PRODUCTINFO/phyCORE-AM57x